REMARKS

Claims 18, 42, and 50 has been cancelled. Claims 19-20, 43-44, and 51 have been amended. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version with markings to show changes made." Claims 1-17, 19-41, 43-49 and 51 are pending.

The drawings stand objected to because Fig. 5 allegedly does not clearly show the connection between the output of the tri-state drivers and the individual bus lines. The Office Action states that the drawing shows the 8 bus lines as a single line while the specification describes each of the tri-state drivers as being connected to only one of the 8 bus lines. The Examiner's attention is directed to small numerals appearing in Fig. 5. For example, referring to portion 40a, the upper tri-state devices each have a "0" at the interconnection between the outputs of the upper tri-state devices and the 8-bit wide Address 0-7 lines, indicating that the output is coupled to bit-0 of the 8-bit wide line. Similarly, the lower tri-state devices each are coupled to different portions of the 8-bit wide "Address 0" line which have numerals 1-7 written at the intersection. These numerals indicate which bit line of the 8-bit wide "Address 0" line is coupled to the tri-state device. This notation also appears for portions 40b ... 40h of the figure. Thus, the information which is alleged to be missing from the Fig. 5 is in fact present in the figure. Figure 5 is drawn in this manner in order to avoid cluttering the figure with 64 lines. Accordingly, the objection to the drawings should be withdrawn.

Applicants are grateful for the acknowledgment of allowable subject matter in claims 9-10, 16-17, 20-21, 30-31, and 38-39. Claim 20 has been rewritten as an independent claims, incorporating all the limitations of its former base and intervening claims. Claim 19 has been amended to depend from claim 20. As such, claim 20, and depending claims 19 and 21 are believed to be allowable over the prior art of record.

Claims 1-8, 11-15, 18-19, 22-29, 32-37, and 40-51 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Fung (U.S. Patent No. 4,380,046). This rejection is respectfully traversed.

Referring to Fig. 2, some computer systems include a main memory 12 which is coupled to both a system CPU 10 via a traditional multi-bit wide bus as well as a massively parallel processing array 14 coupled via a plurality of high speed links to the same main memory 12. The massively parallel processing array 14 typically includes a large plurality of processing elements (PEs) which are arranged as a grid (Fig. 3).

As illustrated in Fig. 4, the plurality of PEs (16a-16n) are typically coupled to the main memory 12 via a corresponding plurality of 1-bit wide data connections 24. Typically, the PEs are designed to read and write data in a vertical direction 30 of the main memory 12. See application at page 4. On the other hand, the CPU 10 of the computer system, accesses the main memory 12 using a traditional multi-bit wide CPU-memory bus and reads and writes the main memory 12 in a horizontal direction 32. See application at page 5. Prior art computer systems therefore must store data in the main memory in accordance with a data format consistent with one direction (e.g., vertically for efficient

access by the array of PEs) and convert the data into another data format consistent with the other direction (e.g., horizontally, for the CPU to transfer between data between main memory and external devices) as necessary depending on what device is accessing the memory. Id. This conversion process may be performed by the PEs, however, the need to convert data format is overhead and reduces the processing throughput of the computer system.

In the present invention the need for the PEs to perform data format conversion is eliminated. Data is stored in the main memory in accordance to one format and if the data must be accessed in another format the conversion is performed "on the fly" by a connection circuit coupled between the PEs and the main memory. See Fig. 5-6. A connection circuit is associated with each PE and includes a plurality of memory buffer registers. The connection circuit can operate in both the horizontal and vertical access modes. In the horizontal access mode, the memory bits are selected so that all bits of a given byte are stored in the same PE (i.e., each set of buffer registers associated with a respective PE contains one byte as seen by the CPU 10 or an external device). In the vertical access mode, each set of buffer registers contains the successive bits at successive locations in the memory corresponding to that PE's position in the memory word. The selection is achieved utilizing a multiplexer on the input to the register and a pair of tri-state drives which drive each data line.

Accordingly, claims 1 and 22 recite: "a main memory" and "a circuit coupled between said main memory and said plurality of processing elements, said circuit writing

data from said plurality of processing elements to said memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements;" claims 11 and 33 recite: "a main memory" and "a plurality of data path circuits, each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements ... wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time." Additionally, claim 41 recites "wherein said step of passing said data further comprises: outputting each bit of said plurality of data bits from said data circuit on a different data bus associated with said memory device; and wherein said step of writing said data further comprises writing said each bit of said plurality of bits data bits to a location in said memory device associated with a different address;" and claim 48 recites "wherein at least a portion of said data is stored in said memory device in a vertical mode."

Fung is directed to a massively parallel processor computer. More specifically, and referring to Fig. 1, Fung discloses a computer system including an array 22 of processing elements 44. The array 22 is also coupled to a CPU 29 via bus 29. Column 5, lines 4-10. Significantly, the computer system of Fung does not require conversion between vertical and horizontal modes of data storage. This is because computer system of Fung lacks a main memory. More specifically, the processing element 44 of Fung (shown in greater detail in Fig. 2) includes a processing circuit (comprising counter/shifter 54,

logic-slider sub-unit 56, and mask sub-unit 58) which is coupled via a bidirectional single bit bus 52 to a local memory unit 50. The natural data format for each PE of Fung is therefore in the horizontal direction. As such, Fig. 2 shows no data conversion circuit interposed between the local memory unit 50 portion and the processing portion of the processing element. Indeed, since the data access performed by the general purpose CPU 26 is also in the horizontal direction, data is never needed or stored in the vertical direction in the computer system disclosed by Fung.

Fung therefore fails to teach or suggest "a main memory" and "a circuit coupled between said main memory and said plurality of processing elements, said circuit writing data from said plurality of processing elements to said memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements" (as required by claims 1 and 22); "a main memory" and "a plurality of data path circuits, each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements ... wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time" (as required by claims 11 and 33); "wherein said step of passing said data further comprises: outputting each bit of said plurality of data bits from said data circuit on a different data bus associated with said memory device; and wherein said step of writing said data further comprises writing said each bit of said plurality of bits

data bits to a location in said memory device associated with a different address" (as required by claim 41); or "wherein at least a portion of said data is stored in said memory device in a vertical mode" (as required by claim 48).

Claims 1, 11, 22, 33, 41, and 48 are therefore believed to be allowable over the prior art of record. Claims 2-10 (which depend from claim 1), 12-17 (which depend from claim 11), 23-31 (which depend from claim 22), 34-40 (which depend from claim 33), 43-47 (which depend from claim 41), and 49 and 51 (which depend from claim 48) are also believed to be allowable for these reasons and because the combination recited in the claims are not taught or suggested by the prior art of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

Please amend claims 19, 20, 41, 43, 44, 48, and 51 as follows:

19. The circuit according to claim 20, [18,] wherein said output of said second tri-sate device is coupled to a different data bus than said output of said first tri-state device.

20. A circuit for connecting a memory device and a processing element of an active memory [The circuit according to claim 18, further] comprising:

a first multiplexer having a first input coupled to said processing element and a second input coupled to a data bus of said memory device;

a first register having an input and an output, said input being coupled to an output of said first multiplexer;

a second multiplexer having an input coupled to said output of said first register and an output coupled to said processing element;

a first tri-state device having an input coupled to said output of said first register and an output coupled to said data bus;

a second tri-state device having an input coupled to said output of said first register and an output coupled to said data bus and a third input of said first multiplexer;

a second register having an input coupled to said output of said first multiplexer;

a third multiplexer having a first input, a second input, and an output, said first input being connected to an output of said second register, said output from said first register being coupled to said second input, said output being coupled to said input of said second multiplexer; and

a fourth multiplexer having a first input, a second input, and an output, said first input being coupled to said output of said first register, said second input being coupled to said output of said second register, said output being coupled to said input of said first and second tri-state devices.

41. A method for writing data from a processing element to a memory device comprising the steps of:

providing a plurality of data bits in a serial manner from said processing element to a data circuit;

passing said data through said data circuit; and

writing said data to said memory device,

wherein said data circuit passes said data directly to said memory device in a horizontal mode[.] and

wherein said step of passing said data further comprises:

outputting each bit of said plurality of data bits from said data circuit on a different data bus associated with said memory device; and

wherein said step of writing said data further comprises writing said each bit of said plurality of bits data bits to a location in said memory device associated with a different address.

43. The method according to claim 41, [42,] wherein said step outputting further comprises:

passing each bit of said plurality of data bits through a respective register.

44. The method according to claim 41, [42,] wherein each different memory address has an associated plurality of bits, and wherein said step of writing each said data bit further comprises:

writing said each bit into a same bit of said associated plurality of bits in each said different memory address.

48. A method for reading data stored in a memory device and providing said data to a processing element, said method comprising the steps of:

providing a plurality of data bits from said memory device to a data circuit;

passing said data through said data circuit; and

outputting said data to said processing element in a serial manner, and

[wherein said data is stored in said memory device in a horizontal mode.]

wherein at least a portion of said data is stored in said memory device in a vertical mode.

51. The method according to claim 48, [50,] wherein said step of passing said at least a portion of said data further comprises:

passing a respective bit of data associated with a different address through a respective register; and

inputting each said respective bit of data associated with said different address to a multiplexer,

wherein said multiplexer outputs said each said respective bit of data in a serial manner to said processing element.